CIS THIN FILM MANUFACTURING AT SHELL SOLAR: PRACTICAL TECHNIQUES IN VOLUME MANUFACTURING

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ABSTRACT

CIS technologies have emerged from the laboratory. Hand crafted construction of a few small devices has given way to practical methods essential to the continuous manufacturing of large modules in high volumes. This paper surveys the present status of CIS production technology as employed at Shell Solar and reviews in detail a number of the methods developed during the transition to volume manufacturing.

INTRODUCTION

CIS products have now been in the marketplace and in the field for several years. CIS modules enjoy a good reputation for high energy delivery and large arrays have been installed, including the world's largest rooptop thin-film PV system, the 245-KWp array on Shell Solar's Camarillo module manufacturing building [1-5].

A number of commercial companies and groups are now manufacturing large power modules and building prototypes using diverse production methods, including direct coevaporation of the semiconductor elements, two-stage processing with reactive annealing, rapid thermal annealing, and even continuous deposition on flexible substrates [4, 6-9]. Even the nomenclature "CIS" encompasses a broad family of thin-film materials: always composed of copper, indium, and selenium but also often containing gallium and/or sulfur.

Previous presentations have focussed on the competitive challenges faced by CIS in a crystalline silicon dominated marketplace and the potential advantages which CIS technologies offer. This report will offer insight into some specific technical problems and solutions for the technology employed for ST-Module production at Shell Solar Industries, and will look ahead at current developments and new products.

CIS MANUFACTURING PROCESS DEVELOPMENT

As previously reported [10], ST-Modules at Shell Solar Industries (SSI) are built from circuits prepared on ordinary low-cost 1x4 foot sodalime glass substrates. The module manufacturing sequence is shown in Figure 1.

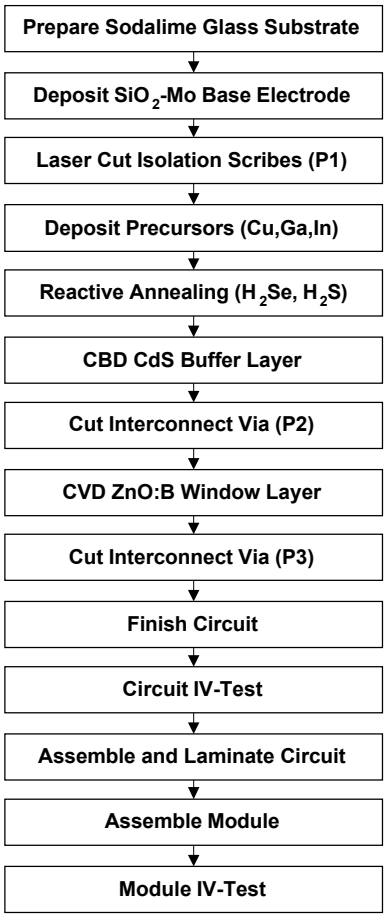


Figure 1. CIS Module Manufacturing Sequence

Specific to the technology employed at SSI are the methods for coating the substrate with barrier and electrode layers, the methods for dosing the growing CIS films with sodium, and the two-stage reactive annealing process. In this section we will elaborate on these key parts of the process.

Base Electrode Requirements

Base electrode coatings are the foundation for high performance thin film cells and modules. For CIS-based devices, molybdenum coatings are virtually universally

used because this refractory metal is highly resistant to reaction with selenium and selenium compounds, making it suitable under a wide range of processing conditions. However, to be practical for module manufacturing, a base electrode structure must also ensure good adhesion of the electrode to the glass substrate, be compatible with the sodium-dosing method employed for CIS-film growth, and be amenable to laser patterning with high scribe quality.

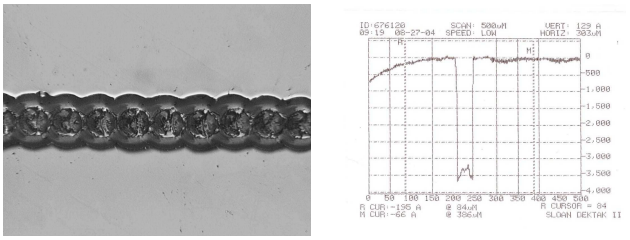
In very early development work at SSI, simple coatings were employed with molybdenum deposited directly on the glass substrates and it was found that molybdenum-to-glass adhesion could be made quite good. Following sputter deposition of the metallic precursor elements, CIS films grown by reactive annealing visually appeared quite uniform. However, adhesion of this CIS to the molybdenum was extremely poor and could not survive CdS CBD processing—when immersed in bath the CIS films would float off of the substrates! SIMS analysis showed a very high concentration of sodium at the CIS-Mo interface. Evidently the hydrogen-rich (H_2Se, H_2S) reaction environment enabled significant ion exchange (H^+ replacing Na^+ in the sodalime substrate) leading to the formation of soluble sodium compounds at this interface. It was clear that the sodium flux from the glass must be reduced.

A number of barrier coatings (sputtered, CVD, even sol-gel) were evaluated before adoption of today's method, the mid-frequency reactive sputtering of SiO_2 from silicon targets. With the insertion of a 50-100nm thick SiO_2 barrier between the glass and molybdenum, excellent adhesion between CIS and molybdenum resulted. And just as important, high circuit efficiency was possible.

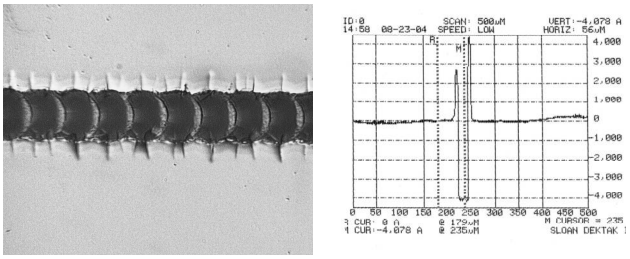
Striking the right sodium "balance" appeared an important goal: some was necessary to achieve good CIS film quality and high circuit efficiency, but too much led to poor adhesion. To this end, experiments were performed and circuits built with SiO_2 thickness varied between 25nm and 400nm. CIS-Mo adhesion was measured using standard ASTM-type tape pull tests with 25 oz-in tapes, performed after deposition of the full CIS/CdS/ZnO device stack (we find this a more stringent test than on CIS alone). Excellent adhesion was generally found to be independent of SiO_2 thickness, although supplementary tests with higher strength tapes suggested slightly better adhesion for the thickest barriers. We believed this demonstrated that the SiO_2 layer was an effective sodium barrier. Circuit and module electrical performance was not only good but, surprisingly, independent of SiO_2 thickness across the whole range investigated. In contrast, we had expected device parameters to vary as sodium flux changed with SiO_2 thickness.

Nevertheless, we concluded that even the thickest barriers must somehow permit out-diffusion of sodium ions sufficient for good CIS quality. We were wrong. The actual mechanism of sodium dosing will be discussed below in the section on reactive annealing.

Good patternability is the third requirement for a base electrode and its importance has been discussed previously [10]. Quality can be judged from optical micrographs and profilometry (Dektak). Examples of good and poor P1 quality are given in Figure 2. Poor quality scribes have a characteristic ragged and partially debonded edge, clearly revealed as a spike at the scribe edge which can cause shunts between ZnO and Mo. In both examples the profilometer depth corresponds to the Mo thickness, showing that the underlying barrier layer remains intact.



Good quality P1 scribe



Poor quality P1 scribe

Figure 2. Examples of P1 Scribe Quality. Optical micrographs (left), Dektak profiles (right).

While scribe quality is influenced by laser set-up, much greater control is offered by choice of molybdenum properties. It is well-known that sputtering pressure strongly influences both stress and resistivity of molybdenum films [11-13]. Lower pressures result in films with lower resistivity and tending toward compressive stress, with higher pressures giving films with tensile stress. Film stress appears to influence the quality of the individual "craters" overlapped to the form scribe line:

- At lower pressure (toward compressive), the craters tend toward smaller diameter with radial cracks apparently defining an extended area of partial delamination.
- At higher pressure (toward tensile), the craters tend to be larger with more jagged and random cracking.

At SSI, good patternability was initially obtained by using a molybdenum bi-layer structure consisting of a thin first layer deposited at low pressure followed by a "bulk" layer deposited at higher pressure, e.g. in a 1:10 thickness ratio at $3x10^{-3}$ and $13x10^{-3}$ mbar respectively. With subsequent development, the cumbersome dual pressure process was replaced by a two-target process at a single pressure ($13x10^{-3}$ mbar) in which the first thin layer was deposited through a honeycomb-form screen, or collimator, to force the molybdenum atom flux into a more

normal angle of incidence, intended to mimic the lower pressure conditions. (Ohring also suggests that a more collimated film would tend toward compressive stress [13]). Empirically, tuning the bilayer conditions allows control of the scribe quality and balancing film layer stresses appears to underlie this result. More recent refinements [10] established an additional control parameter: pattern quality could be tuned by the addition of a small amount of oxygen to the argon sputter gas (in the range 2-15%) for deposition of the first, thin layer. (Deposition conditions for the bulk layer are unaltered and isolation slits between the separate target compartments minimize cross contamination).

Precursor Process Improvements

Our earlier presentations have discussed methods for controlling the critical Cu / (In + Ga) ratio, especially in view of variability and drift of deposition rates with target aging, particularly for indium [10, 14]. Through cooperation with target vendors, they were able to use our production experience to develop improvements in target fabrication methods so that the drift in deposition rate is nearly negligible over the life of the target. While the process control methods outlined earlier [14] are still employed, the frequency of control measurements and adjustments could be reduced.

Machine utilization was significantly improved with the implementation of XRF measurements of the precursor layers. Using this non-destructive tool, control measurements could be made on production substrates rather than special quartz crystal carriers, increasing productivity by as much as 40%.

Reactive Annealing and Sodium Dosing

The Shell Solar batch reactive annealing process has been described previously [10]. In short, metal precursor films are selenized by reaction with H_2Se and subsequently sulfurized by reaction with H_2S. The reactors hold up to 25 substrates loaded parallel with the precursor coatings facing the uncoated rear side of the adjacent substrate. We now know that most, and possibly all, of the sodium incorporated into the final CIS film originated in the adjacent sodalime glass surface, not in the substrate on which the CIS is grown.

The incorporation appears to occur in three steps. First, reaction of H_2Se with sodalime glass (SLG), exchanging protons for sodium cations.

$$2\,Na^+_{(glass)} + H_2Se \rightarrow Na_2Se_{(s)} + 2H^+_{(glass)} \qquad (1)$$

Second, the sublimation of the sodium selenide formed by reaction (1).

$$Na_2Se_{(s)} \rightarrow Na_2Se_{(v)} \qquad (2)$$

Finally, the transport (diffusion, convection) of sodium selenide vapor (2) to the growing CIS surface and its incorporation into the CIS film.

$Na_2Se_{(v)}$ reaction with growing CIS film (3)

The reactivity of SLG can be demonstrated directly by simultaneous selenization of different substrate types: after processing, quartz and 7059 substrates show no appreciable coating while SLG substrates are distinctly coated with selenium dust, the oxidized residue of Na_2Se. If examined immediately after selenization, a SLG substrate is coated with a cloudy white substance (Na_2Se) which turns an orange-red color (elemental Se) upon exposure to air, matching the properties and reactivity described by Gmelin [15].

Even in the earliest research experiments, it became apparent that devices made on the outermost substrate*, whose CIG film did not face another substrate,* systematically yielded Voc some 50mV lower than the others.

To explore this effect, standard runs were done with conventional loading of 1x4 substrates, except:

- One 1x4 was reversed, so its CIG film faced the CIG film of the adjacent 1x4.
- One 1x4 was replaced by an SLG sheet coated on both sides with a SiO_2 barrier layer, so the CIG film of the adjacent 1x4 faced a barrier-coated SLG surface.

Circuit test	CIG facing SLG	CIG facing CIG	CIG facing SiO_2/SLG
Voc (V)	0.524	0.474	0.459
Jsc (mA/cm^2)	34.9	28.2	29.1
FF	0.572	0.322	0.330
Eff (%)	10.5	4.3	4.4

Table 1. Effect on 1x4 circuit performance of the surface adjacent to the CIG film during reactive annealing.

The effect is dramatic, affecting all parameters on 1x4 circuits while only Voc was suppressed on small (e.g. 10x30cm) substrates, suggesting that Na_2Se diffusion has a limited range.

SIMS analysis of representative samples offers further insight. To probe the extent of diffusion from sources other than the adjacent facing surface, e.g. from a substrate's own rear side, samples were diced from positions at the mid-point of the substrate's 4-foot length and at several locations from top to bottom along the 1-foot axis: about 3cm from the top and bottom edges and about 3cm above and below the middle. Sodium depth profiles of all samples exhibited typical [16] qualitative features: enrichment at the CIS surface, a relatively lower concentration in the bulk of the CIS with concentration increasing toward a maximum at the CIS-Mo interface.

Beyond the qualitative similarity, the quantitative differences between samples and between different positions within a sample are striking. Data from the profiles are summarized in Figures 3 and 4, showing that sodium concentrations are suppressed by an order of magnitude in the middle of the 1x4 substrate and less so near the edges, again evidence that diffusion from sodium sources other than the adjacent facing surface is limited.

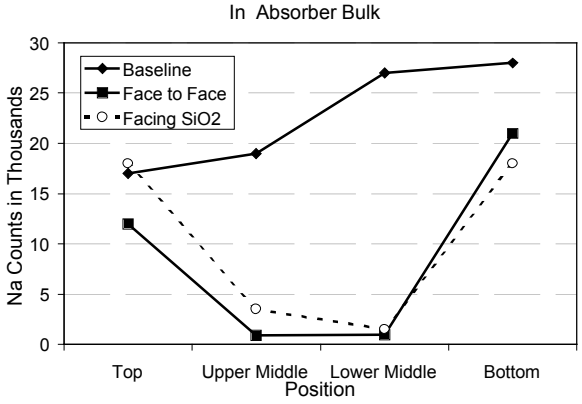


Figure 3. Sodium concentrations in CIS absorber bulk

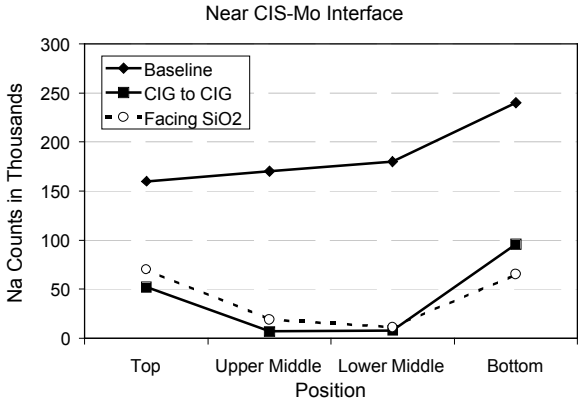


Figure 4. Sodium concentrations near the CIS-Mo interface

In production a practical solution is employed: the outward facing substrate is omitted and replaced with an SLG sheet so that the next inboard substrate also faces an uncoated SLG surface. The effect diminishes after 1-2 runs so this "sacrificial" SLG is replaced each run.

The Shell Solar reactive annealing process enjoys simple, inherent sodium dosing. However, there could be disadvantages: the initial reaction (Eq. 1) and subsequent sublimation (Eq. 2) are surely temperature dependent. Increased batch sizes increase temperature gradients during reactive annealing. External sodium dosing could produce better uniformity, especially for larger batches. The next section will discuss the newest work with this option.

REACTIVE ANNEALING AND SPUTTER DOSING OF SODIUM

Very recently we have combined the sodium sputter dosing process developed by our Munich R&D colleagues [16] with our standard batch reactive annealing process. Precursor substrates were prepared with the baseline process, except that a sodium compound was sputtered onto the base electrode. All substrates were loaded in pairs with CIG films facing CIG films to minimize conventional sodium dosing during reactive annealing. Figure 5 shows the results from this first trial.

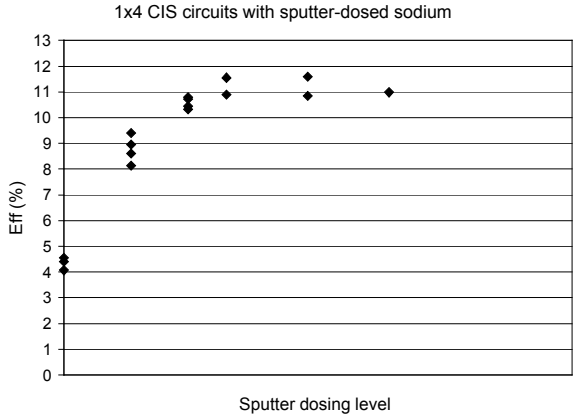
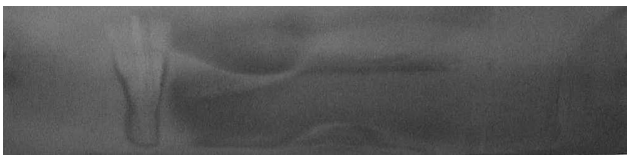


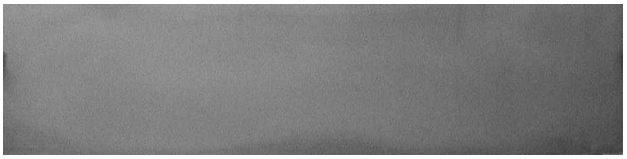
Figure 5. Performance of 1x4 circuits vs. sodium sputter dosing level

Efficiency increases steadily with increased dosing with all parameters (Voc, Jsc, FF) exhibiting the same trend. CIS-Mo adhesion also improved with increased dosing through the range examined. At present, with tuning of reactive annealing conditions, average 1x4 module performance has improved from the 40W baseline to 42.4W using sputter dosing (11% to 11.7% aperture efficiency). This work is continuing, as is additional work to investigate higher dosing levels.

First trials also confirmed that sodium sputter dosing could produce better uniformity across the 1x4 substrate for larger reactive annealing batches. During batch reactive annealing, the innermost substrates experience the largest temperature gradients, an effect magnified by larger batch sizes. With conventional precursors, the CIS produced exhibits significant nonuniformity easily visible as dark and light bands and spots, illustrated in Figure 6. In contrast, CIS produced from sputter-dosed precursors is extremely uniform.



CIS from conventional precursors



CIS from precursors with sodium sputter dosing

Figure 6. CIS film uniformity produced by reactive annealing under conditions with large temperature gradients.

NEW PRODUCTS AND DESIGNS

As discussed previously, simplified glass-glass module packaging offers a major opportunity for cost reduction but implementation was hindered by breakage at the solder and ribbons during lamination [6]. This key obstacle has now been eliminated by incorporation of a standard glazing seal material [17], illustrated in Figure 7. The seal material supports the glass edges during lamination, preventing any bending or breakage across the solder ribbon. Further, it conveniently prevents EVA leakage, eliminating the need for post-lamination trimming.

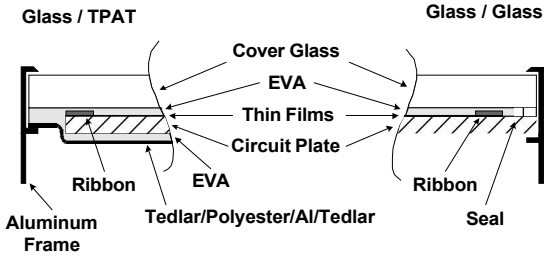


Figure 7. Current CIS package design using TPAT (left) and new glass / glass design with edge seal (right).

Equally important, the seal material has excellent dielectric properties and moisture resistance, even after 1000 hours of Damp Heat (85°C/85%RH) exposure. In-house testing of this design shows no evidence of humidity penetration into the circuit until at least 2000 hours of exposure, even on unframed laminates.

This concept provides the basis for a new product under development, the ST80. Illustrated in cross-section in Figure 8, this nominally 80W module will incorporate two 1x4 circuits laminated to a single cover glass. A small printed circuit board built into the laminate connects the circuits in series (parallel is also possible) and places terminals at a point convenient for J-box attachment. The cover glass can optionally be screen printed on the interior surface with a black frit perimeter like those used on automobile windshields to provide an even more aesthetically pleasing appearance.

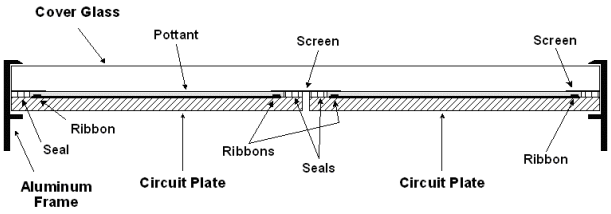


Figure 8. New ST80 module design

Figure 9 shows the IV-curve of one of the first several complete prototypes.

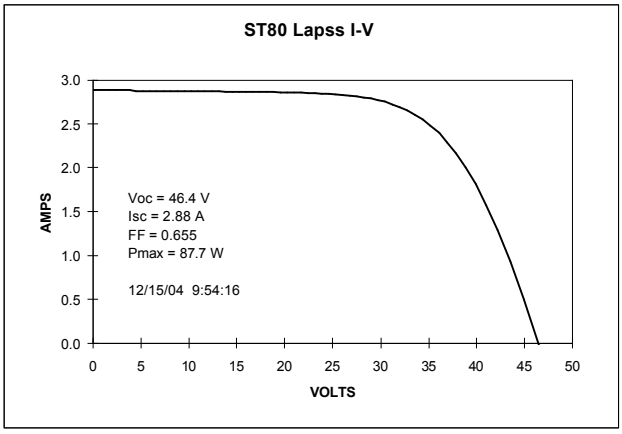


Figure 9. IV-curve of early ST80 prototype

CONCLUSIONS

A number of the new techniques necessary for volume manufacturing have been reviewed and some of the newest developments have been presented, including design and test results for a new high power CIS module. We believe that CIS technologies have significant potential for performance and cost improvements.

ACKNOWLEGEMENTS

This work was supported in part by the National Renewable Energy Laboratory (NREL), Golden, CO, under subcontract No. ZDJ-2-30630-16 of the Thin Film Photovoltaic Partnership Program. The authors are especially grateful to Sally Asher and Matthew Young of NREL for their terrific responsiveness and help with SIMS profiles and analysis. The authors also wish to recognize former CIS colleagues C. Fredric, C. Jensen, and S. Voss for their important contributions to the work presented here.

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